

SSC8132GN1

N-Channel Enhancement Mode MOSFET with ESD protection

Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	I _D	ESD
30V	+20V	560mΩ@5V0	0.5A	1K
30 V	ZOV	720mΩ@2V75	0.57	

Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

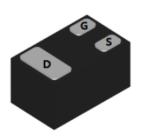
Applications

- Load Switch
- Portable Devices

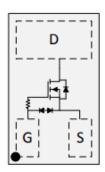
Ordering Information

Device	Package	Shipping	
SSC8132GN1	DFN1006-3L	10000/Reel	

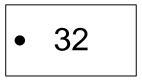
> Pin configuration



DFN1006-3L (Bottom View)



Pin Configuration (Top View)



Marking

Analog Future



➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	30	V
Gate-to-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current a	I _D	0.5	А
Pulsed Drain Current b	I _{DM}	3	Α
Power Dissipation ^c	P _D	0.8	W
Operation junction temperature, Storage temperature range	T _J , T _{STG}	-55 to 150	$^{\circ}$ C

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
Reja	Junction-to-Ambient Thermal Resistance a	160	°C/W

Note:

- a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with T_A =25 °C. The value in any given application depends on the user is specific board design. The current rating is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

SSC-V1.1 www.sscsemi.com Analog Future



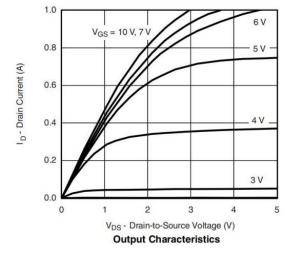


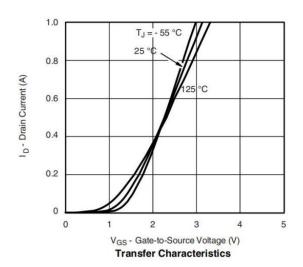
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

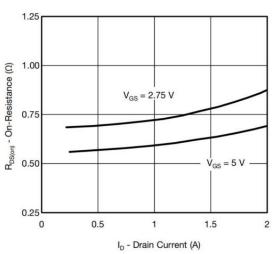
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250uA$	0.5	1	1.5	V
Drain Sauras On Basistanas	_	V _{GS} = 5V, I _D = 0.5A		560	730	m0
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 2.75V, I _D = 0.3A		720	950	mΩ
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 20V, V_{DS} = 0V$			±10	μA
Transconductance	stance G_{FS} $V_{DS} = 25V$, $I_D = 0.2A$		100			ms
Forward Voltage	V _{SD}	V _G S = 0V, I _S = 0.2A		0.8	1.4	V
Input Capacitance	C _{ISS}	\		45		
Output Capacitance	Coss	$V_{DS} = 15V$, $V_{GS} = 0V$, $f = 1MHz$		12		pF
Reverse Transfer Capacitance	C _{RSS}	I = IIVIDZ		4.5		
Total Gate Charge	Q _G	V 00V V 5V		0.8		
Gate Source Charge	Q _{GS}	V _{DS} = 20V, V _{GS} = 5V,		0.1		nC
Gate Drain Charge	Q _{GD}	$I_D = 0.2A$		0.53		
Turn-on Delay Time	T _{D(ON)}	$V_{GS} = 5V$, $V_{DS} = 30V$,		20		no
Turn-off Delay Time	$T_{D(OFF)}$	$R_G = 3\Omega$, $I_D = 0.2A$		20		ns

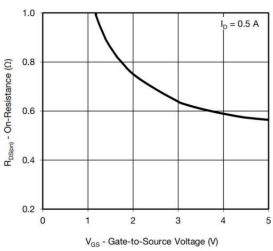


➤ Typical Performance Characteristics (T_A=25°C unless otherwise noted)



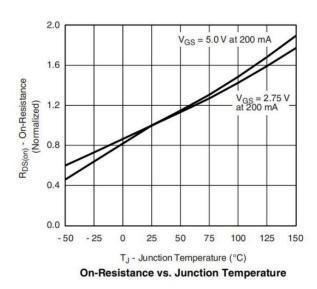


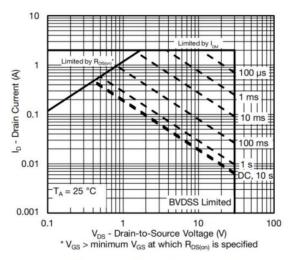




On-Resistance vs. Drain Current

On-Resistance vs. Gate-to-Source Voltage



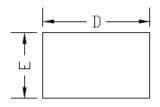


Safe Operating Area, Junction-to-Ambient

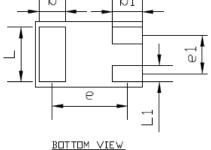


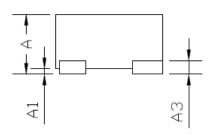
Package Information

POD



TOP VIEW

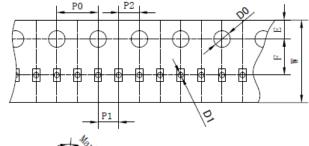




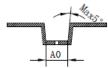
SIDE VIEW

COMMON DIMENSION (MM)						
PKG	DFN1006					
REF.	MIN.	MAX				
Α	>0.4	-	0,50			
A1	0,00	_	0.05			
A3	0.125REF.					
D	0.95	1.00	1.05			
E	0.55	0.60	0.65			
b	0.20	0.25	0.30			
b1	0.20	0.30	0.40			
L	0.45	0.50	0.55			
L1	0.10	0.15	0,20			
е	0.675					
e1	0,35					

Tape Data







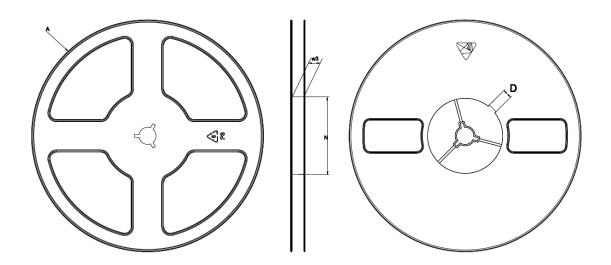
SYMBOL	A0	ВО	КО	P0	P1	P2
SPEC	0.69±0.05	1. 15±0. 05	0.60±0.05	4.00±0.10	2.00±0.05	2.00±0.05
SYMBOL	T	E	F	DO	D1	W
SPEC	0.18±0.03	1.75±0.10	3.50±0.05	1.55±0.05	0.50±0.05	8.00 +0.5

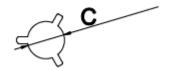
NOTE:

- 1. 材料: 黑色防静电材料;
- 2.10个链孔的累积公差不能超过±0.2
- 3. 尺寸符合EIA-481-E的要求。



Reel Data





材质说明:该产品用料为 □ □ □

TYPE	Α	N	С	D	w3
8MM	+1 Ø178 -1	+1 Ø60-1	+0,3 Ø13,3-0,3	7,5±0,5	9±0.3



DISCLAIMER

SSCSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. SSCSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.

OUR PRODUCT SPECIFICATIONS ARE ONLY VALID IF OBTAINED THROUGH THE COMPANY'S OFFICIAL WEBSITE, CRM SYSTEM, OR OUR SALES PERSONNEL CHANNELS. IF CHANGES OR SPECIAL VERSIONS ARE INVOLVED, THEY MUST BE STAMPED WITH A QUALITY SEAL AND MARKED WITH A SPECIAL VERSION NUMBER TO BE VALID.

SSC-V1.1 <u>www.sscsemi.com</u> Analog Future